WHAT IS CLAIMED IS:

1. A computer implemented method of multilevel dither screening comprising the steps of:

defining a dither value for each pixel of a screening matrix;

packing plural pixel values corresponding to plural pixels into equal sections of a first data word;

packing plural corresponding dither values into said equal sections of a second data word;

adding corresponding sections said first data word and said second data word in an arithmetic logic unit selectively spilttable into said equal sections forming a sum data word;

saturating any section of said sum data word generating an carry output during addition to a section of all 1's forming a saturated sum data word; and

truncating a predetermined number of least significant bits of each section of said saturated sum data word forming a dither screen data word.

2. The method of claim 1, wherein:

said step of adding corresponding sections said first data word and said second data word further includes saving a carry out of each section in a multiple flags data word;

said step of saturating any section of said sum data word generating an carry output during addition includes

expanding said carry out of each section in said multiple flags data word to fill a corresponding section of a mask data word,

forming the logical OR of (1) a logical AND of a saturated data word having all 1's in every section and said mask data word, and (2) a logical AND of said sum data word and a logical inverse of said mask data word.

3. The method of claim 1, wherein:

said step of truncating a predetermined number of least significant bits of each section of said saturated sum data word includes

right shifting said saturated sum data word said predetermined number of bits,

forming a mask data word having said predetermined number of 1's in least significant bits of each section and 0's in most significant bits of each section, and

forming a logical AND of said shifted saturated sum data word and said mask data word.

4. The method of claim 1, wherein:

said input pixel values are represented in a fixed point format of 8 bits including 4 integer bits and 4 fractional bits;

said dither values are represented in a fixed point format of 4 bits including zero integer bits and 4 fractional bits; and

said predetermined number of bits is 4.

5. The method of claim 1, further comprising the step of:

quantizing each section of said dither screen data word into a limited set of threshold ranges.

6. A printer comprising:

a transceiver adapted for bidirectional communication with a communications channel;

a memory;

a print engine adapted for placing color dots on a printed page according to received image data and control signals; and

a programmable data processor connected to said transceiver, said memory and said print engine, said programmable data processor including a selectively splittable arithmetic logic unit, said programmable data processor programmed to:

receive print data corresponding to pages to be printed from the communications channel via said transceiver;

convert said print data into image data and control signals for supply to said print engine for printing a corresponding page, said conversion including multilevel dither screening by

defining a dither value for each pixel of a screening matrix,

packing plural pixel values corresponding to plural pixels into equal sections of a first data word,

packing plural corresponding dither values into said equal sections of a second data word,

adding corresponding sections said first data word and said second data word in said arithmetic logic selectively spilt into said equal sections forming a sum data word,

saturating any section of said sum data word generating an carry output during addition to a section of all 1's forming a saturated sum data word, and

truncating a predetermined number of least significant bits of each section of said saturated sum data word forming a dither screen data word.

7. The printer of claim 6, wherein:

said programmable data processor further including

a multiple flags register connected to said arithmetic logic unit receiving and storing a carry out from each of said sections of said arithmetic logic unit, and

an expand circuit connected to said multiple flags register for expanding each bit of said multiple flags register to fill a corresponding section thereby forming a mask data word; and

wherein said programmable data processor is programmed to saturate any section of said sum data word generating an carry output during addition by

forming in said arithmetic logic unit the logical OR of (1) a logical AND of a saturated data word having all 1's in every section and said mask data word, and (2) a logical AND of said sum data word and a logical inverse of said mask data word.

8. The printer of claim 6, wherein:

said programmable data processor further including

a selectable shifter,

a mask generator having an input and an output filling each section with a number of least significant 1's equal to a number at said input and

wherein said programmable data processor is programmed to truncating a predetermined number of least significant bits of each section of said saturated sum data word by

supplying said predetermined number to said shifter to right shift said saturated sum data word by said predetermined number of bits,

supplying said predetermined number to said input of said mask generator thereby forming a mask data word having said predetermined number of 1's in least significant bits of each section and 0's in most significant bits of each section, and

forming in said arithmetic logic unit a logical AND of said shifted saturated sum data word and said mask data word.